

UNITED STATES PATENT APPLICATION

**H<sub>2</sub> PLASMA TREATMENT**

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## **H<sub>2</sub> PLASMA TREATMENT**

### **Cross Reference To Related Applications**

This application is related to commonly assigned U.S. patent application,  
5 Micron no. 02-1122, serial no. \_\_\_\_\_, filed on 15 April 2003, entitled  
“Improved Surface Barriers for Copper and Silver Interconnections Produced by a  
Damascene Process,” which is hereby incorporated by reference in its entirety.

### **Technical Field**

10 This application relates generally to semiconductor devices and device  
fabrication, and more specifically to fabricating metals in a damascene structure.

### **Background**

One of the main problems confronting the semiconductor processing  
15 industry, in the ULSI age, is that of capacitive-resistance loss in the wiring levels.  
This has led to a large effort to reduce the resistance of and lower the capacitive  
loading on wiring levels. Since its beginning, the industry has relied on aluminum  
and aluminum alloys for wiring. In a like manner, the industry has mainly relied on  
SiO<sub>2</sub> as the insulator of choice, although polyimide was used in a number of  
20 products by IBM, for a number of years. The capacitive resistance problem grows  
with each succeeding generation of technology.

To improve the conductivity, it has been suggested to substitute copper,  
silver or gold metallurgy for the aluminum metallurgy now being used. Several  
potential problems have been encountered in the development of these proposed  
25 metallurgies. One problem is the fast diffusion of copper through both silicon and  
SiO<sub>2</sub>. This problem, along with the known junction poisoning effects of copper and  
gold, have led to proposals to use a liner to separate these metallurgies from an SiO<sub>2</sub>  
insulator. These approaches, however, do not fully resolve problems associated  
with decreasing minimum line size and decreasing liner size. The combination of

the shrinking line size in the metal line and the decreasing liner size increases both the capacitance and resistance.

With respect to capacitive loading effects, studies have been conducted that considered employing various polymers such as fluorinated polyimides as possible  
5 substitutions for SiO<sub>2</sub> insulators. Several of these materials have dielectric constants considerably lower than SiO<sub>2</sub>. However, as in the case of SiO<sub>2</sub>, an incompatibility problem with copper metallurgy has been found. In the case of polyimide, and many other polymers, it has been found that the polymer, during curing, reacts with copper during the curing process, forming a conductive oxide CuO<sub>2</sub>, which is  
10 dispersed within the polymer. See, D. J. Godbey et al., International Conference on Metallurgical Coatings and Thin Films, San Diego, CA, Abstract H2.04, pg. 313 (April 21-25, 1997). This conductive oxide then raises the effective dielectric constant of the polymer and in many cases increases the polymers conductivity.

Various approaches using copper and other metals in SiO<sub>2</sub> and polymer  
15 insulators have been implemented to improve the properties of the electrical interconnects. However, these electrical characteristics are impaired when an oxide is formed at or near the surface of the electrical interconnect. Thus, structures and methods are needed which alleviate the problems associated with via and metal line fabrication processes.

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### Summary

The above mentioned problems are addressed by the present invention and will be understood by reading and studying the following specification. An embodiment for a method for forming an electronic device includes forming a first  
25 conductive layer in an opening in a multilayer dielectric structure supported by a substrate, forming a core conductive layer on the first conductive layer, subjecting the core conductive layer to a H<sub>2</sub> plasma treatment, and depositing a capping adhesion/barrier layer on the core conductive layer after the H<sub>2</sub> plasma treatment. In an embodiment, the multilayer dielectric structure provides an insulating layer  
30 around the core conducting layer and at least one sacrificial layer for processing.

The H<sub>2</sub> plasma treatment removes unwanted oxide from the surface region of the core conducting layer such that the interface between the core conducting layer and the capping adhesion/barrier is substantially free of oxides. In an embodiment, the core conducting layer is copper with a titanium nitride or zirconium capping  
5 adhesion/barrier layer.

These and other aspects, embodiments, advantages, and features will become apparent from the following description and the referenced drawings.

### **Brief Description of the Drawings**

10 Figures 1A-1H illustrate elements for an embodiment of a process to form metallizations, according to various embodiments of the present invention.

Figures 2A-2I illustrate elements for another embodiment of a process to form metallizations, according to various embodiments of the present invention.

Figure 3A shows an embodiment of a process element for forming a  
15 wiring/metallization structure, according to the teachings of the present invention.

Figure 3B shows another embodiment of a process element for forming a wiring/metallization structure, according to the teachings of the present invention.

Figure 4 is a simplified block diagram of a memory device using an  
20 embodiment for a wiring structure according to the teachings of the present invention.

Figure 5 illustrates a block diagram for an embodiment of an electronic system having devices using a wiring structure according to the teachings of the present invention.

### **Detailed Description**

25 The following detailed description refers to the accompanying drawings that show, by way of illustration, specific aspects and embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention. Other embodiments  
30 may be utilized and structural, logical, and electrical changes may be made without

departing from the scope of the present invention. The various embodiments disclosed herein are not necessarily mutually exclusive, as some disclosed embodiments can be combined with one or more other disclosed embodiments to form new embodiments.

5           The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form an integrated circuit (IC). The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and  
10       substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art.

          The term “horizontal” as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the  
15       orientation of the wafer or substrate. The term “vertical” refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as “on”, “side” (as in “sidewall”), “higher”, “lower”, “over” and “under” are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed  
20       description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

          In various embodiments, an electronic device using layered metallizations in a wiring structure is produced by a method that includes forming within an insulator  
25       a conductive structure having a core conductor layer on a first conducting layer and a capping adhesion and/or barrier (adhesion/barrier) layer on the core conductor layer, where the capping adhesion/barrier layer is formed on the core conductor layer after subjecting the core conductor layer to a H<sub>2</sub> plasma treatment. Subjecting the core conductor layer to a H<sub>2</sub> plasma treatment prior to forming the capping  
30       adhesion/barrier layer provides an interface between the core conductor and the

capping adhesion/barrier that is substantially free of an oxide. As a result, the conductive structure can provide improved metallizations for an integrated circuit in which the surface of the metallization layer is substantially free of an oxide or sub-oxide. In an embodiment, the first conducting layer includes an adhesion/barrier  
5 layer and a seed layer. In a further embodiment, the structure produced may be an air bridge. In an embodiment, the insulator is a polyimide layer. In another embodiment, the insulator is an oxide layer. In an embodiment, the core conducting layer is a copper layer.

The use of a copper conductor along with a barrier/liner layer provides  
10 significant improvement in conductivity over a Ti/AlCu/Ti sandwich structure now in widespread use in the microelectronics industry. However, as the line width decreases even a thin liner has a significant effect on the composite line resistance. As minimum dimensions shrink, the use of even a twenty angstrom layer of an alloy with higher resistivity will have a significant effect on the total resistivity of the  
15 conductor composite. See, P.C. Andricacos, *The Electrochemical Society Interface*, pp. 32-37, (Spring 1999).

It has also been shown that there is a significant difference between the amount of copper oxide that is formed when a polyimide insulator is used if the acidity of the polymer solution is low, i.e., if the precursor used in the formation of  
20 the polyimide is an ester instead of an acid. In the case of PI-2701, which is a photosensitive polyimide that starts from an ester precursor, the amount of oxide formed is reduced by a factor of approximately four as compared to films with a similar final chemistry, prepared from an acid precursor. It is thought that the slight acidity of PI-2701 may come from the photo-pac or the process used to form it.

25 The use of Ti as a barrier layer was found to increase the resistivity of a Cu film significantly when heat-treated at temperatures of 350°C or above. However, if the heat-treatment was carried out in hydrogen no increase in resistivity was reported. As this temperature is above the eutectoid temperature of the TiH system, the formation of TiH is assumed to have occurred. A similar increase in resistivity  
30 was reported to occur with Zr-containing and Hf-containing copper alloys. See, S.P.



*Muraka et al., SPIE, vol. 2335, pp. 80-90.* From the equilibrium phase diagrams of the Cu-Ti and Cu-Zr systems, it can be seen that the solubility of Zr in Cu is more than ten times less than that of Ti.

In addition to copper, gold and silver also offer lower resistivities than  
5 aluminum. These materials also have a significantly lower adhesion to oxides than aluminum. These materials as well as aluminum have relatively poor adhesion to polymers. Processes that offer significant improvements to the barrier adhesion art for the bottom and the sidewall damascene or dual damascene structures are provided by the present inventor in U.S. patent 6,376,370 issued 23 April 2002, U.S.  
10 patent 6,420,262 issued 30 July 2002, U.S. patent 6,426,289 issued 16 July 2002, and U.S. patent application, Micron no. 02-1122, serial no. \_\_\_\_\_, filed on 15 April 2003, which are hereby incorporated by reference.

In various embodiments according to the teachings of the present invention, the formation of a capping adhesion/barrier layer on the top surface of a damascene  
15 metal is preceded by subjecting the top surface of the damascene metal to a H<sub>2</sub> plasma treatment. This eliminates or substantially reduces the probability of forming an oxide or sub-oxide on the top surface of the core conductor of the damascene metal between the time that the core conductor is deposited and the time that the capping adhesion/barrier layer is formed. The formation of such an oxide or  
20 sub-oxide would decrease the adhesion of the top barrier to the underlying metallurgy, and also increase the resistivity of the interface.

In embodiments according to the present invention, methods in a damascene process provide for eliminating or substantially reducing top layer oxides or sub-oxides without increasing a capping adhesion/barrier thickness. Prior to the  
25 deposition of the capping adhesion/barrier, a H<sub>2</sub>-containing plasma is used to reduce the metal oxides on the top surface. The plasma treatment may either be performed in the deposition chamber in which the capping adhesion/barrier layer is formed or in a separate chamber of a multi-chamber deposition system. In an embodiment, conductive material is deposited to form a capping adhesion/barrier layer by a low  
30 energy ion implant. The ion implant energy employed provides depositing the bulk

of the implanted material in the top few atomic layers. The resulting structure can be exposed to a nitrogen-containing plasma or to an elevated temperature nitrogen treatment, forming a conducting nitride layer on the metal surfaces.

Figures 1A-1H illustrate elements for an embodiment of a process to form metallizations for an electronic device at various processing stages. Figure 1A illustrates a portion of an integrated circuit structure, namely an integrated circuit having a number of semiconductor devices formed in a substrate. Figure 1A further illustrates the structure after a device structure is formed in the substrate and the contact structure to the device structure is in place. One of ordinary skill in the art will understand upon reading this disclosure the manner in which a number of semiconductor structures, e.g. transistors, can be formed in a substrate. For example, Figure 1A illustrates the structure after a number of device structures, e.g. transistor 101A and 101B are formed in the substrate 100. An insulator layer 102 is deposited over the number of semiconductors 101A and 101B. In an embodiment, insulator layer 102 includes a field oxide 102A and a layer 102B of  $\text{Si}_3\text{N}_4$ . In an embodiment, insulator layer 102 includes a layer of  $\text{Si}_3\text{N}_4$  having a thickness of about 100 Angstroms ( $\text{\AA}$ ). This insulator layer will also serve as an additional barrier to impurities coming from subsequent processing steps.

Contact holes 105A and 105B are opened to the number of device structures 101A and 101B using a techniques that are known to those skilled in the art. In an embodiment, TiN layers 106A, 106B are deposited followed by deposition of tungsten layers 107A, 107B by a process such as chemical vapor deposition (CVD) to form contact plugs. Other conducting materials may be used. Excess tungsten and TiN are removed from the  $\text{Si}_3\text{N}_4$  surface by chemical mechanical planarization (CMP) or other suitable processes to form a planarized surface 109.

As shown in Figure 1B, a multilayer dielectric structure having a lower insulator layer 108, an intermediate dielectric layer 103, and a top dielectric layer 104 is deposited over the wafer surface. In an embodiment, each layer 108, 103, 104 is deposited independently over the wafer surface. Lower insulator 108 will provide the insulating layer in which a conducting structure will be formed, while



intermediate dielectric layer 103 and top dielectric 104 provide sacrificial layers for the fabrication process. In an embodiment, lower insulator layer 108 is deposited over the  $\text{Si}_3\text{N}_4$  layer 102B and the contact plugs formed in vias 105A, 105B. Lower insulator layer 108 is deposited with a thickness equal to the wiring at that level.

5 In an embodiment, lower insulator layer 108 is a polymer, a fluorinated polymer, or a foamed polymer. A polymer layer 108 can be deposited using, for example, the process and material disclosed in U.S. patent 6,284,656 issued 4 September 2001, hereby incorporated by reference. Following deposition of a polymer, it is cured. In an embodiment, lower insulator layer 108 includes a  
10 polyimide layer, a fluorinated polyimide layer, or a foamed polyimide layer. In an embodiment, lower insulator 108 is a polyimide layer applied to surface 109 such that when cured it will have sufficient thickness to equal the thickness for a first wiring level. Polyimide layer 108 may be converted to a foamed polyimide by a method, for example, that uses a supercritical fluid as described in U.S. patent  
15 6,077,792 issued 20 June 2000, hereby incorporated by reference.

In an embodiment, a low temperature oxide is deposited as intermediate layer 103 having a thickness of about 500Å. A layer of  $\text{Si}_3\text{N}_4$  having a thickness of about 500Å is deposited as top dielectric 104 on intermediate layer 103. Other thicknesses may be used. A thin layer of resist is applied to top dielectric layer 104.  
20 The required damascene images are etched in the oxide layer 103 and the nitride layer 104. To define trenches in polyimide layer 108, an  $\text{O}_2$  reactive ion etching (RIE) process is used, which also removes the thin resist layer. Thus polyimide layer 108, or lower insulator 108, is patterned to define a trench 110, or a number of trenches, in the lower insulator layer 108 providing an opening to first level vias,  
25 107A and 107B, or a number of vias, in planarized surface 109. The structure is now as appears in Figure 1C.

As shown in Figure 1D, an adhesion/barrier layer 114 is deposited in trench 110, or the number of trenches, using a low energy ion implantation. In an embodiment, adhesion/barrier layer is formed by another method such as by CVD.  
30 In an embodiment, adhesion/barrier layer 114 includes a layer of zirconium having a

thickness of approximately 5 to 100 Å. In alternate embodiments, adhesion/barrier layer 114 includes a layer of titanium and/or hafnium. In one embodiment, layer 114 of zirconium has a thickness of approximately 50 Å. This can be achieved using a  $10^{17}$  ion implant of zirconium, i.e.  $10^{17}$  ions of zirconium per square centimeter ( $\text{cm}^2$ ). In an embodiment, the layer of zirconium 114 is implanted at 100 electron volts (eV) into the surface of the trenches 110 in polymer layer 108 using a varying angle implant ( $\alpha$ ), as represented by arrows 111, where the angle of implantation is changed from normal to the wafer surface to 15 degrees off normal. As one of ordinary skill in the art will understand upon reading this disclosure, using a varying angle implant, where an angle of implantation is changed from normal to planarized surface 109 to approximately 15 degrees off normal, deposits adhesion/barrier layer 114 on all surfaces in trench 110, or in the number of trenches. Also, in forming adhesion/barrier layer 114, various refractory metals can be employed, such as tantalum, tungsten, molybdenum, hafnium, niobium, rhenium, osmium, ruthenium, zirconium, titanium, vanadium, chromium and manganese. In various embodiments, alloys of Ta or W with N or with certain polyimides, in particular, those formed from the ester of Zr, Ti or Hf, are employed. The structure is now as appears in Figure 1D.

In Figure 1E, a seed layer 116 is deposited on adhesion/barrier layer 114. In an embodiment, seed layer is deposited using a low energy ion implantation at energies ranging from 100 electron volts (eV) to 2000 electron volts (eV). In another embodiment, seed layer is deposited by CVD. In various embodiments, seed layer 116 on adhesion/barrier layer 114 includes a layer of aluminum, copper, silver, or gold. Seed layer 116 serves as a catalyst or base metal for subsequent electroless plating or electroplating of a core conducting layer and as an adhesion layer preventing delamination of subsequently electrolessly deposited or electroplated metal. In various embodiments, seed layer 116 includes a layer of one or more refractory metals such as tantalum, tungsten, molybdenum, hafnium, niobium, rhenium, osmium, ruthenium, zirconium, titanium, vanadium, chromium and manganese. In an embodiment, a copper seed layer is utilized for a core

conducting layer of copper. In an embodiment, seed layer 116 includes a layer of copper having a thickness of approximately a 100 Å. This can be achieved using an  $8 \times 10^{16}$  ion implant of copper using a low energy ion implantation. The resulting structure is shown in Figure 1E.

5           After seed layer 116 is deposited,  $\text{Si}_3\text{N}_4$  layer 104 is removed using a selective etch. An etchant is selected that negligibly attacks polyimide layer 108 and oxide layer 103. The selective etch also removes seed layer 116 and adhesion/barrier layer 114 from all areas except in the trench 110. Alternately, seed layer 116 and adhesion/barrier layer 114 along with silicon nitride layer 104 may be  
10 removed from the surface by a chemical mechanical planarization (CMP) process stopping on the oxide layer 103. The structure is now as shown in Figure 1F.

          In Figure 1G, a core conducting layer 120, or a number of first level metal lines 120, is deposited over the seed layer 116 in trench 110, or in a number of trenches. Core conducting layer, or number of first level metal lines 120, is a layer  
15 substantially of aluminum, copper, silver, or gold depending on the type of seed layer 116 deposited. Core conducting layer 120 is electrolessly plated into trench 110 on seed layer 116 to a thickness which causes core conducting layer 120 to extend to about the level of a top surface 119 of polyimide layer 108. Electroless metal deposition is attractive due to low processing costs and high quality metal  
20 deposits. In addition, equipment for performing electroless metal deposition is relatively inexpensive compared to other semiconductor processing equipment for depositing metals. Electroless deposition also provides for batch processing wafers, thereby further reducing cost and increasing production throughput. In an embodiment, copper is electroless plated onto seed layer 116. In an embodiment,  
25 forming conductive layer 120 includes electroless plating copper in an ambient air environment. Electroless copper plating is used to deposit sufficient copper to fill trench 110, or a number of trenches, to top surface 119 of polyimide insulator layer 108.

          Core conducting layer 120 is subjected to a  $\text{H}_2$  plasma treatment. This  
30 removes unwanted oxide from the surface of core conducting layer 120. With

respect to Figure 1H, the surface of core conducting layer 120 is then implanted with material to form a capping adhesion/barrier layer 122 to prevent metal contamination. In various embodiments, the capping is a material such as aluminum, boron, chromium, molybdenum, tungsten, titanium, zirconium, hafnium, magnesium, vanadium, columbium, or tantalum or oxides or nitrides of these elements. In an embodiment, core conducting layer is copper and the dopant is zirconium. The zirconium is implanted at an energy level of about 0.125 keV to 2.0 keV and at a concentration of about  $1.25 \times 10^{16}$  ions/cm<sup>2</sup> to about  $2.0 \times 10^{17}$  ions/cm<sup>2</sup>. In an embodiment, the zirconium is implanted at an energy of about 0.5 keV and at a concentration of about  $5 \times 10^{16}$  ions/cm<sup>2</sup>. In other embodiments using other dopants, the implant energy and the concentration can range from about 0.125 to about 2.0 keV and from about  $1.25 \times 10^{16}$  to about  $2 \times 10^{17}$  ions/cm<sup>2</sup>, respectively. In an embodiment, capping adhesion/barrier layer ranges from about 5 Å to about 40 Å thick. In an embodiment, capping adhesion/barrier layer is around 20 Å thick.

Oxide layer 103 is removed by an etch which attacks oxide but has no or negligible effect on polyimide. This removes the capping layer from all areas except on core conducting layer 120. In an embodiment, this etch removes zirconium from all areas except from capping adhesion/barrier layer 122 on copper core conducting layer 120. The resulting capping adhesion/barrier layer 122 can be utilized in an interconnect system for an integrated circuit coupling passive and/or active components such as capacitors, transistors and various memory devices. The resulting structure is shown in Figure 1H.

The formation of the metallization structure as discussed with respect to Figures 1A-1H describes a single damascene structure, other implementations using dual damascene can be constructed using appropriate masking steps. The process is then repeated as many times as necessary to build the multi-level wiring layers desired. Depending upon the temperatures used in the processes for applying and curing the polymers as well as depositing the resist stack, a final post processing heat-treatment of about 250°C to about 350°C for about one hour to about two hours may be used to reduce the resistivity of the conductors in the wiring structure. If an

air bridge structure is desired all or a portion of the polymer insulation can be removed by subjecting the completed structure, or a portion thereof, to an oxygen plasma treatment.

Figures 2A-2I illustrate elements for another embodiment of a process to form metallizations for an electronic device at various processing stages. Figure 2A illustrates a portion of an integrated circuit structure, namely an integrated circuit having a number of semiconductor devices formed in a substrate. Figure 2A further illustrates the structure after a device structure is formed in the substrate and the contact structure to the device structure is in place. For example, Figure 2A illustrates the structure after a number of device structures, e.g. transistor 201A and 201B are formed in the substrate 200. An insulator layer 202 is deposited over the number of semiconductors 201A and 201B. In an embodiment, insulator layer 202 includes a field oxide 202A and a layer 202B of  $\text{Si}_3\text{N}_4$ .  $\text{Si}_3\text{N}_4$  layer 202B may be formed on or below field oxide 202A. In an embodiment, insulator layer 202 includes a layer of  $\text{Si}_3\text{N}_4$  having a thickness of about 100 Å. This insulator layer will also serve as an additional barrier to impurities coming from subsequent processing steps.

Contact holes 205A and 205B are opened to the number of device structures 201A and 201B using a techniques that are known to those skilled in the art. In an embodiment, TiN layers 206A, 206B are deposited followed by deposition of tungsten layers 207A, 207B by a process such as chemical vapor deposition (CVD) to form contact plugs. Other metals may be employed to form contact plugs. Excess tungsten and TiN are removed from the  $\text{Si}_3\text{N}_4$  surface by chemical mechanical planarization or other suitable processes to form a planarized surface 209.

As shown in Figure 2B, a multilayer dielectric structure having a lower insulator layer 208 and a top dielectric layer 204 is deposited over the wafer surface. In an embodiment, each layer 208, 204 is deposited independently over the wafer surface. Lower insulator 208 will provide the insulating layer in which a conducting structure will be formed, while top dielectric 204 provides a sacrificial layer for the



fabrication process. In an embodiment, lower insulator layer 208 is deposited over the  $\text{Si}_3\text{N}_4$  layer 202B and the contact plugs formed in vias 205A, 205B. Lower insulator layer 208 is deposited with a thickness equal to the wiring at that level.

In an embodiment, lower insulator layer 208 is a oxide, a fluorinated oxide, or an aerogel. In an embodiment, lower insulator layer 208 is a silicon oxide layer. In an embodiment, lower insulator layer 208 is a silicon dioxide layer. Referring to Figure 2B, lower insulator layer 208 having a top surface 219 is deposited with a thickness equal to the wiring at that level. In an embodiment, a layer of  $\text{Si}_3\text{N}_4$  having a thickness of about 500Å is deposited as top dielectric 204 on lower insulator layer 208. Other thicknesses may be used. A thin layer 203 of resist is applied to  $\text{Si}_3\text{N}_4$  layer 204.

The required damascene images are etched in the resist 203 and the nitride layer 204. To define trenches in oxide layer 208, an oxide etch is used, which also removes the remaining resist layer. Thus oxide layer 208, or lower insulator 208, is patterned to define a trench 210, or a number of trenches, in the oxide layer 208 providing an opening to first level vias, 207A and 207B, or a number of vias, in planarized surface 209. The structure is now as appears in Figure 2C.

As shown in Figure 2D, an adhesion/barrier layer 214 is deposited in trench 210, or in the number of trenches, using a low energy ion implantation. In an alternate embodiment, adhesion/barrier layer is formed by another method such as by CVD. In an embodiment, adhesion/barrier layer 214 includes a layer of zirconium having a thickness of approximately 5 to 100 Å. In alternate embodiments, adhesion/barrier layer 214 includes a layer of titanium and/or hafnium. In one embodiment, layer 214 of zirconium has a thickness of approximately 50 Å. This can be achieved using a  $10^{17}$  ion implant of zirconium, i.e.  $10^{17}$  ions of zirconium per square centimeter ( $\text{cm}^2$ ). In an embodiment, the layer of zirconium 214 is implanted at 100 electron volts (eV) into the surface of the trenches 210 in the oxide layer 208 using a varying angle implant ( $\alpha$ ), as represented by arrows 211, where the angle of implantation is changed from normal to the wafer surface to 15 degrees off normal. Using a varying angle implant, where



an angle of implantation is changed from normal to the planarized surface 209 to approximately 15 degrees off normal deposits the adhesion/barrier layer 214 on all surfaces in trench 210, or in the number of trenches. Also, in various embodiments, in forming the adhesion/barrier layer 214, refractory metals can be employed, such as tantalum, tungsten, molybdenum, hafnium, niobium, rhenium, osmium, ruthenium, zirconium, titanium, vanadium, chromium and manganese. In some embodiments, alloys of Ta or W with N, Zr, Ti, or Hf are employed. The structure is now as appears in Figure 2D.

In Figure 2E, a seed layer 216 is deposited on adhesion/barrier layer 214. In an embodiment, seed layer is deposited using a low energy ion implantation at energies ranging from 100 electron volts (eV) to 2000 electron volts (eV). In another embodiment, seed layer 216 is deposited by CVD. In various embodiments, seed layer 216 on adhesion/barrier layer 214 includes a layer of aluminum, copper, silver, or gold. Seed layer 216 serves as a catalyst or base metal for subsequent electroless plating or electroplating of a core conducting layer and as an adhesion layer preventing delamination of subsequently electrolessly deposited or electroplated metal. In various embodiments, forming the seed layer includes forming a layer of one or more refractory metals such as tantalum, tungsten, molybdenum, hafnium, niobium, rhenium, osmium, ruthenium, zirconium, titanium, vanadium, chromium and manganese. In an embodiment, a copper seed layer is utilized for a core conducting layer of copper. In an embodiment, seed layer 216 includes a layer of copper having a thickness of approximately a 100 Å. This can be achieved using an  $8 \times 10^{16}$  ion implant of copper using a low energy ion implantation. The structure is now as shown in Figure 2E.

After seed layer 216 is deposited, if the fill is to be electroplating, the plating process is performed. Following electroplating the material deposited upon the surface of the wafer is removed, by chemical mechanical polishing, stopping on the silicon nitride. If electroless plating is to be used the seed/barrier layer deposited on the surface of the wafer is removed by chemical mechanical polishing stopping on the nitride layer. This removes portions of adhesion/barrier layer 214 and seed

layer 216 that were deposited on the resist layer 203, leaving adhesion/barrier layer 214 and seed layer 216 extending only in the trench 210 to approximately the level of the top surface of  $\text{Si}_3\text{N}_4$  layer 204 (top dielectric layer 204). The structure is shown in Figure 2F. In an alternate embodiment, when barrier and seed layers 214 and 216 are removed,  $\text{Si}_3\text{N}_4$  layer 204 is also removed.

In Figure 2G, a core conducting layer 220, or a number of first level metal lines 220, has been deposited over seed layer 216 in trench 210, or in a number of trenches. Core conducting layer 220, or number of first level metal lines 220, may be a layer of aluminum, copper, silver, or gold depending on the type of seed layer 216 deposited. Core conducting layer 220 is electrolessly plated into trench 210 on seed layer 216 to a thickness which causes the metal layer 220 to extend to about the level of a top surface 219 of oxide layer 208. In an embodiment, copper is electroless plated onto seed layer 216. In an embodiment, forming conductive layer 220 includes electroless plating copper in an ambient air environment. Electroless copper plating is used to selectively deposit copper with a thickness slightly less than the thickness of oxide layer 208, that is, the nominal copper thickness plus the deposition tolerance equals the thickness of oxide layer 208.

Core conducting layer 220 is subjected to a  $\text{H}_2$  plasma treatment. This removes unwanted oxide from the surface of core conducting layer 220. Referring to Figure 2H, the surface of core conducting layer 220 is then implanted with dopant to form a capping adhesion/barrier layer 222 to prevent metal contamination. In various embodiments, the dopant is a material such as aluminum, boron, chromium, molybdenum, tungsten, titanium, zirconium, hafnium, magnesium, vanadium, columbium, or tantalum or oxides or nitrides of these elements. In an embodiment, core conducting layer is copper and the dopant is titanium. Titanium is implanted at an energy of about 0.5 keV and at a concentration of about  $5 \times 10^{16}$  ions/cm<sup>2</sup>, penetrating the copper core conducting layer 220 to an average depth of about 10 Å. In an embodiment, the titanium is implanted at an energy level of about 0.125 keV to 2.0 keV and at a concentration of about  $1.25 \times 10^{16}$  ions/cm<sup>2</sup> to about  $2.0 \times 10^{17}$  ions/cm<sup>2</sup>. In other embodiments using other dopants, the implant energy and the

concentration can range from about 0.125 to about 2.0 keV and about  $1.25 \times 10^{16}$  to about  $2 \times 10^{17}$  ions/  $\text{cm}^2$ , respectively. In an embodiment, capping adhesion/barrier layer ranges from about 5 Å to about 40 Å thick. In an embodiment, capping adhesion/barrier layer is around 20 Å thick.

5           In a Ti ion implantation process in which Ti ions penetrate through  $\text{Si}_3\text{N}_4$  layer 204 and are implanted into oxide layer 204, a region of dielectric material containing  $\text{TiO}$ ,  $\text{TiO}_2$ , and/or  $\text{TiO}_x$  is formed in oxide layer 204. In an alternate process in which  $\text{Si}_3\text{N}_4$  layer 204 is removed when removing resist layer 203, during  
10           implanting into copper layer 220 titanium is also implanted into oxide layer 208 at an average distance of about 20 Å using an implant energy of about 0.5 keV. In other embodiments, the titanium is deposited using other deposition processes as alternatives to ion implantation.

          Capping adhesion/barrier layer 222 may be exposed to a nitrogen to form a conducting nitride on core conducting layer 220. In an embodiment, titanium layer  
15           222 is exposed to a nitrogen plasma at 350°C to form a TiN layer 222 on copper core conducting layer 220. With a region of oxide layer 204 containing  $\text{TiO}_x$ , a nitrogen exposure process may form a region containing  $\text{TiO}$ ,  $\text{TiO}_2$ , and/or a  $\text{TiO(N)}_x$ . The structure with conducting layer 220 having capping adhesion/barrier layer 222 is shown in Figure 2H. In an embodiment in which oxide layer 208  
20           having implanted titanium is exposed to nitrogen plasma, a  $\text{TiO}$ ,  $\text{TiO}_2$ , and/or a  $\text{TiO(N)}_x$  layer is formed on oxide layer 208.

          In embodiments in which  $\text{Si}_3\text{N}_4$  layer 204 is present during formation of capping adhesion/barrier layer 222,  $\text{Si}_3\text{N}_4$  layer 204 (top dielectric layer 204) is then removed with negligible effect on oxide layer 208. In an embodiment,  $\text{Si}_3\text{N}_4$  layer  
25           204 is removed by an etchant, such as hot phosphoric acid ( $\text{H}_3\text{PO}_4$ ) at a temperature of about 180°C at a etch rate of about 80 Å/min., which selectively attacks the top dielectric layer 204 and not the oxide layer 208. Any TiN formed in  $\text{Si}_3\text{N}_4$  layer 204 is removed leaving first oxide layer 208 free of impurities (i.e. TiN). In addition, the remaining part of the conducting layer containing adhesion/barrier layer 214 and  
30           seed layer 216 not in contact with core conducting layer 220 and capping

adhesion/barrier layer 222 is removed along with the removal of  $\text{Si}_3\text{N}_4$  layer 204. This structure is shown in Figure 2I. The resulting core conducting layer 220 and capping adhesion/barrier layer 222 can be utilized in an interconnect system for an integrated circuit coupling passive and/or active components such as capacitors, transistors, various memory devices, and various electronic devices and systems.

The formation of the metallization structure as discussed with respect to Figures 2A-2H describes a single damascene structure, other implementations using dual damascene can be constructed using appropriate masking steps. The process is then repeated as many times as necessary to build the multi-level wiring layers desired.

Figure 3A shows an embodiment of a process element for forming a wiring/metallization structure. Figure 3A illustrates a multilayer dielectric structure 307 supported by a substrate 300 in which a damascene structure is formed. Multilayer dielectric structure 307 includes a lower insulator layer 308, an intermediate dielectric layer 303, and a top dielectric layer 304 disposed over a wafer surface. Lower insulator 308 will provide the insulating layer in which a conducting structure will be formed, while intermediate dielectric layer 303 and top dielectric 304 provide sacrificial layers for the fabrication process. In various embodiments, a number of different dielectrics can be used to realize each of these layers 308, 303, 304. In an embodiment as shown in which Figure 3A, the multilayer dielectric structure 307 is formed over a contact plug 302. In this embodiment, contact plug 302 has at least a portion of its body above supporting substrate 300, rather than completely in a contact hole. From the stage of the process shown in Figure 3A, an embodiment for a processing method includes forming a first conductive layer in an opening that has been formed in the multilayer dielectric structure 307, forming a core conductive layer on the first conductive layer, subjecting the core conductive layer to a  $\text{H}_2$  plasma treatment, and depositing a capping adhesion/barrier layer on the core conductive layer after the  $\text{H}_2$  plasma treatment. In an embodiment, lower insulating layer 308 is a polymer layer. The structure for an embodiment shown in Figure 3A can be processed as previously

described for a polymer insulating layer, including a polyimide insulating layer, with respect to Figures 1B-1H.

Figure 3B shows another embodiment of a process element for forming a wiring/metallization structure. Figure 3B illustrates a multilayer dielectric structure 317 supported by a substrate 310 in which a damascene structure is formed. Multilayer dielectric structure 317 includes a lower insulator layer 318, and a top dielectric layer 314 disposed over a wafer surface. Lower insulator 318 will provide the insulating layer in which a conducting structure will be formed, while top dielectric 314 provides a sacrificial layer for the fabrication process. In various embodiments, a number of different dielectrics can be used to realize each of these layers 318, 314. In an embodiment as shown in which Figure 3B, the multilayer dielectric structure 317 is formed over a contact plug 312. In this embodiment, contact plug 312 has at least a portion of its body above supporting substrate 310, rather than completely in a contact hole. From the stage of the process shown in Figure 3B, an embodiment for a processing method includes forming a first conductive layer in an opening that has been formed in the multilayer dielectric structure 317, forming a core conductive layer on the first conductive layer, subjecting the core conductive layer to a H<sub>2</sub> plasma treatment, and depositing a capping adhesion/barrier layer on the core conductive layer after the H<sub>2</sub> plasma treatment. In an embodiment, lower insulating layer 318 is an oxide layer. The structure for an embodiment shown in Figure 3B can be processed as previously described for an oxide insulating layer with respect to Figures 2B-2I.

Figure 4 is a simplified block diagram of a memory device 400 using an embodiment for wiring structure according to the teachings of the present invention. Memory device 400 includes an array of memory cells 402, address decoder 404, row access circuitry 406, column access circuitry 408, control circuitry 410, and input/output (I/O) circuit 412. The memory is operably coupled to an external microprocessor 414, or memory controller for memory accessing. Memory device 400 receives control signals from processor 414, such as WE\*, RAS\* and CAS\* signals, which can be supplied on a system bus. Memory device 400 stores data that



is accessed via I/O lines. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device of Figure 4 has been simplified to help focus on embodiments of the present invention. At least one of the structures associated with memory device 400 uses a wiring structure in a substrate in accordance with an embodiment of the present invention.

It will be understood that the above description of a memory device is intended to provide a general understanding of the memory and is not a complete description of all the elements and features of a specific type of memory, such as DRAM (Dynamic Random Access Memory). Further, embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to the DRAM described above. Other alternative types of devices include SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs and other emerging DRAM technologies.

Figure 5 illustrates a block diagram for an embodiment of an electronic system 500 having devices using a wiring structure according to the teachings of the present invention. Electronic system 500 includes a controller 505, a bus 515, and an electronic device 525, where bus 515 provides electrical conductivity between controller 505 and electronic device 525. In various embodiments, controller 505 and/or electronic device 525 includes an embodiment for a wiring structure as discussed herein. In an embodiment, electronic system 500 includes a plurality of electronic devices using an embodiment for a wiring structure according to the present invention. Electronic system 500 may include, but is not limited to, information handling devices, wireless systems, telecommunication systems, fiber optic systems, electro-optic systems, and computers.

Applying a H<sub>2</sub> plasma treatment to a core conducting layer in a damascene structure prior to forming a capping adhesion/barrier layer on the core conducting



layer provides a method for removing unwanted oxides and sub-oxides from the surface of the core conducting layer. Electronic devices and systems constructed having metallizations using such a process are provided with interconnection metallizations with enhanced conductivity properties. These enhanced conductivity (reduced resistivity) properties are provided in part by a interconnection structure in which the interface between the core conducting layer and a capping adhesion/barrier layer is substantially free of oxides. Embodiments for methods in line with the embodiments described herein provide for the use of highly conducting metals such as copper and silver. In embodiments, these copper or silver structures are insulated using polymer layers or oxide layers that can be fabricated in a variety of different forms such as, but not limited to, foamed materials or fluorinated materials.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments, will be apparent to those of skill in the art upon reviewing the above description. The scope of the present invention includes any other applications in which the above structures and fabrication methods are used. The scope of the present invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.